Amendments to the Claims:

The following listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) A high-voltage PMOS transistor comprising:

an insulated gate electrode;

a p-conductive source region in an n-conductive well which is arranged on a p-conductive substrate;

a p-conductive drain region in a p-conductive well which is arranged in said n-conductive well, said drain region having a portion facing away from said n-conductive well and forming part of a plane corresponding to an upper surface of the transistor; and

an insulation area between said gate electrode and said drain region;

wherein ~~the depth of~~ a lower boundary of the n-conductive well extends a shorter distance into the p-conductive substrate away from the upper surface underneath said drain region ~~is less~~ than the lower boundary of the n-conductive well extends into the p-conductive substrate away from the upper surface underneath said source region, and ~~the depth of~~ a lower boundary of the p-conductive well extends a farther distance into the n-conductive well away from the upper surface ~~being greatest~~ underneath said drain region than the lower boundary of the p-conductive well extends into the n-conductive well away from the upper surface underneath a region lateral to said drain region.

2. (Previously Presented) The high-voltage PMOS transistor as claimed in claim 1, wherein the p-conductive well extends laterally from the drain to the gate electrode.

3. (Currently Amended) The high-voltage PMOS transistor as claimed in claim 1, wherein the gate electrode extends above an insulating layer from the source region as far as [[the]] a field oxide in the direction of the drain so that it covers the edge areas of the p-conductive well.

4. (Currently Amended) The high-voltage PMOS transistor as claimed in claim 1, wherein a field plate including a metal layer extends at a predefined distance above [[the]] a field oxide and is connected to the gate electrode by means of a via, and in that the metal layer extends over the field oxide [[area]] from the gate electrode in the direction of the drain.

5. (Previously Presented) The high-voltage PMOS transistor as claimed in claim 1, wherein the p-conductive well is more highly doped in the vicinity of the drain than in the external area towards the transistor channel (K).

6. (Previously Presented) The high-voltage PMOS transistor as claimed in claim 1, wherein the n-conductive well has lower doping underneath the drain than in the area underneath the transistor channel.

7. (Withdrawn) A mask for manufacturing an n-conductive well of a high-voltage PMOS transistor, in which the area of the drain which is provided is covered with a drain cover,

and a further cover between the areas which are provided for the drain and the source is produced at a distance from the drain cover.

8. (Canceled)

9. (Withdrawn) The mask as claimed in claim 7, wherein the further cover is embodied in a strip shape.

10. (Withdrawn) The mask as claimed in claim 7, wherein the drain cover is firstly widened in the vicinity of the transistor head (TK) and then tapers.

11. (Withdrawn) The mask as claimed in claim 7, wherein the drain cover extends in an arc in the vicinity of the transistor head (TK).

12. (Withdrawn) The mask as claimed in claim 7, wherein the further cover follows the profile of the drain cover in the vicinity of the transistor head, at a distance.

13. (Withdrawn) A masking for manufacturing a p-conductive well of a high-voltage PMOS transistor in which additional covers are provided in certain sections between the central area (Z) and the edge area of the well which is to be produced, which widen in the direction from the source which is provided to the drain which is provided, and are spaced apart from one another.

14. (Withdrawn) The masking as claimed in claim 13, wherein the additional covers contain conically extending strips.

15. (Withdrawn) The masking as claimed in claim 13, wherein the additional covers are formed in the vicinity of the transistor head as strips which are spaced apart from one another.

16. (Withdrawn) The masking as claimed in claim 14, wherein the strip-shaped additional covers are a plurality of strips which extend in an arc.

17. (Withdrawn) The masking as claimed in claim 14, wherein the strips extend in parallel at least in certain sections.

18. (Withdrawn) A method for manufacturing an n-conductive well and a p-conductive well of a high-voltage PMOS transistor having a p-conductive drain region in the p-conductive well which is arranged in the n-conductive well, in which the implantation of ions is carried out by means of masks or maskings in such a way that the doping depth of the p-conductive well is greater under the drain which is provided than in the direction of the well areas which are assigned to the source.

19. (Withdrawn) The method as claimed in claim 18, wherein the local conductivity of the p-conductive well is also determined by the doping of the n-conductive well.

20. (Withdrawn) The method as claimed in claim 18, wherein the well masking is carried out for the p-conductive well in such a way that the depth of the n-conductive well is less in the area of the drain which is provided than in the other well areas.